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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/646,103
Filing Date: August 22, 2003
Appellant(s): LIU ET AL.

Michael S. Okamoto, reg. No. 47,831
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 9/1/2006 appealing from the Office action mailed 4/19/2005.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The following are the related appeals, interferences, and judicial proceedings known to the examiner, which may be related to, directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal:

U.S. Patent Application No. 10/873,363, filed on June 21, 2004, currently under appeal No. 20063363.

(3) Status of Claims

The statement of the status of claims contained in the brief is incorrect. A correct statement of the status of the claims is as follows:

This appeal involves claims 1-7.

Claims 8-20 are allowed.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is substantially correct. The changes are as follows:

WITHDRAWN REJECTIONS

The following grounds of rejection are not presented for review on appeal because they have been withdrawn by the examiner:

A) Rejection of independent claim 8 under 35 U.S.C § 102(b) as being anticipated by Tehrani.

B) Rejection of independent claim 12 under 35 U.S.C. § 102(b) as being anticipated by Tehrani.

C) Rejection of dependent claims 9, 13, 14, 16, 17, 19, and 20 under 35 U.S.C. § 102(b) as being anticipated by Tehrani.

D) Rejection of dependent claims 10, 11, 15, and 18, under 35 U.S.C. § 103(a) as being unpatentable over Tehrani in view of Yue.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

5,861,328	TEHRANI	1-1999

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 1, 2, and 4 are rejected under 35 U.S.C. 102(b) as being anticipated by Tehrani (US 5861328).

Regarding claim 1, Tehrani shows (see, *e.g.*, figs. 4-8) all aspects of the instant invention including a process for passivating a magneto-resistive bit **41** having a top surface and side walls characterized by encapsulating the top and side wall surfaces of the bit **41** with a conductive etch stop barrier layer.

Regarding claim 2, Tehrani shows the conductive barrier layer comprising CrSi (see, *e.g.*, col.6/ll.1).

Regarding claim 4, Tehrani shows the method further comprising forming a diffusion barrier between the conductive barrier layer and the top surface and sidewalls of the bit (see, *e.g.*, col.6/ll.2).

Claims 3 and 5-7are rejected under 35 U.S.C. 103(a) as being unpatentable over Tehrani in view of Yue (US 5496759).

Regarding claim 3, Tehrani shows most aspects of the instant invention (see, *e.g.*, paragraphs above). He, however, fails to specify the thickness of the etch-stop layer. However, differences in thickness will not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such thickness and/or concentration are critical. "Where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the workable ranges by routine experimentation". *In re Aller*, 220 F.2d 454,456,105 USPQ 233, 235 (CCPA 1955).

Since the applicants have not established the criticality (see next paragraph) of the etch-stop thickness, and since the claimed thickness of 300 Å is in common use in similar devices in the art (see, *e.g.*, Yue/col.2/ll.42), it would have been obvious to one of ordinary skill in the art to use these values in the device of Tehrani.

CRITICALITY

The specification contains no disclosure of either the critical nature of the claimed thickness or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the applicant must show that the chosen dimensions are critical. *In re Woodruff*, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Regarding claim 5, Tehrani shows the diffusion barrier comprises Ta (see, *e.g.*, col.6/ll.2).

Regarding claims 6, Yue shows the diffusion barrier is about 100 Å (see, *e.g.*, col.2/ll.40). See also the comments stated about with respect to claim 3, which are considered repeated here.

Regarding claim 7, Tehrani shows the diffusion barrier comprises TaN (see, *e.g.*, col.6/ll.2).

(10) Response to Argument

The appellants argue:

> Tehrani teaches two distinct processes, a process with a dielectric barrier and a process suitable for a conductive etch stop barrier layer, but only illustrates the process with the dielectric barrier in the figures. The examiner is improperly mixing the teachings of the process suitable for the conductive barrier (not illustrated) with the teachings of the process with the dielectric barrier (illustrated). The claimed invention requires sidewalls of a magnetoresistive bit to be encapsulated by a conductive etch stop barrier layer. The examiner applied a conductive barrier teaching of Tehrani and improperly combines it with another Tehrani process in which sidewalls of a bit are exposed prior to forming a dielectric barrier. In fact the two processes are separate and incompatible. The first process with the dielectric barrier is illustrated in figures 5, 6, and 7 and described in col.4/ll.66-col.5/ll.53. In said first process via openings 47 and 50 are formed in separate operations. The second process with the conductive barrier is described in col.5/ll.54-col.6/ll.12 and it is not shown. In said second process the vias 47 and 50 are formed in a single operation. Tehrani explicitly teaches that two distinct processes are taught by the use of the term "either" in col.6/ll.13-14, which indicates two exclusive alternatives.

The examiner responds:

Tehrani is using his figures to describe both processes. Otherwise, why would Tehrani use the same reference numbers to refer to the same features in his description of both processes? The examiner agrees with the appellants that Tehrani uses figures 5-8 to describe the first process. Tehrani, however, does not provide any other figures, besides figures 5-8, in his description of the second process, yet he uses the same reference numbers (see, *e.g.*, col.5/ll.54-col.6/ll.12). That the figures referred to both processes is evinced in the fact that Tehrani uses the same reference numbers in his

description of both processes and that he clearly indicates so when referring to figure 8 as applying to both processes (see, *e.g.*, col.6/ll.13-17).

In any event, Tehrani clearly sets forth what are the differences between both processes. That is, in the first process vias 47 and 50 are formed in separate steps, as illustrated in figures 6 and 7 (see, *e.g.*, col.5/ll.22-35), whereas in the second process vias 47 and 50 are formed in a single operation (see, *e.g.*, col.5/ll.54-55). In that regard, figures 6 and 7 will be particular to the first process but only for their showing of forming vias 47 and 50 in two separate method steps. In any event, "[A]fter the formation of vias 47 and 50, by either of the above described means" (see, *e.g.*, col.6/ll.13-14), both processes will continue, "[a]s illustrated in FIG. 8" (see, *e.g.*, col.6/ll.16-17).

The appellants argue:

> Tehrani admonishes against a combination of the two processes. With respect to the first process via openings 50 may overlap GMR element 41, that is, vias 50 may extend outside or intersect the end of the GMR element 41 (see, *e.g.*, col.5/ll.36-38). In contrast, with respect to the second process, Tehrani states that via openings 50 must be enclosed by GMR element 41, that is, the contact may not extend outside the ends of the GMR memory 41 to protect element 41 from the resist stripping processes and other oxidizing or corrosive agents (see, *e.g.*, col.5/ll.58-62).

The examiner responds:

Tehrani clearly sets forth the differences between the two processes. Setting forth the differences between the two processes is not the same as admonishing against combining both processes. The two processes are very similar to each other with one step difference. In the first process, vias 47 and 50 are formed in separate steps (see, *e.g.*, col.5/ll.34-35). In the second process vias 47 and 50 are formed in a single operation (see, *e.g.*, col.5/ll.54-55). In the first process, because of the requirements to protect the bit, the vias 47 are formed first (see, *e.g.*, col.5/ll.25-27). Subsequent to forming the vias 47, the vias 50 are formed (see, *e.g.*, col.5/ll.35).

Because Tehrani uses two separate steps to form vias 47 and 50 in the first process, the etching of vias 50 is customized allowing the vias to extend outside the bit 41 (see, *e.g.*, figs. 6-7 and col.5/ll.25-38). That is because the chemistries used to etch vias 50 in the first process are gentle enough not to damage or corrode the bit 41 (see, *e.g.*, col.5/ll.48-50). On the other hand, in the second process, Tehrani combines forming vias 47 and 50 in one single operation. Now that vias 47 are formed together with vias 50, Tehrani restrict forming the vias 50 so that the contacts may not extend outside the ends of the bit to better protect the bit 41 (see, *e.g.*, col.5/ll.54-62).

That both processes are very similar to each other is evinced in the fact that Tehrani clearly indicates that "[A]fter the formation of vias 47 and 50, by either of the above described means" (see, *e.g.*, col.6/ll.13-14), both processes will continue, "[a]s illustrated in FIG. 8" (see, *e.g.*, col.6/ll.16-17).

The appellants argue:

> Tehrani teaches two distinct processes, the first process uses a dielectric barrier and the second process uses a conductive barrier. In the first process Tehrani uses silicon nitride as a barrier layer, a second SiO_2 layer, and an optional third layer of AlO or AlN as an etch stop layer for the dielectric cap 45 (see, *e.g.*, col.5/ll.3-21). None of these materials are conductive. In the second process he uses CrSi as a conductive barrier layer.

The examiner responds:

Tehrani teaches that the cap layer 45 is a dielectric layered system and he specifically refers to it as the dielectric cap layer 45 in his description of both processes (see, *e.g.*, col.5/ll.4 and col5/ll.57-58). The first layer of this dielectric cap 45 completely seals the bit structure 41 and provides a barrier to moisture, oxidation, and corrosive agents (see, *e.g.*, col.5/ll.4-8 and figure 5). This is also illustrated in figure 5, where Tehrani shows the cap layer 45 sealing the bit structure 41. The difference between the

cap layer of the first and second processes is that the first layer of the dielectric cap 45 in the second process is a conductive etch stop barrier layer (see, *e.g.*, col.5/ll.55-58 and col.5/ll.67-col.6/ll.2).

The appellants argue:

> In the second process, Tehrani states that vias 50 must be enclosed by GMR element 41, *i.e.*, that the contact may not extend outside the ends of bit 41. As he further describes, where the etch stop and passivation layer is conductive, contact metal can be simply deposited in contact therewith in vias 50 (see, *e.g.*, col.6/ll.9-12). Thus, when Tehrani describes a conductive etch stop barrier layer, the layer explicitly does not encapsulate the sidewalls.

The examiner responds:

The two processes are very similar to each other with one step difference. In the first process, vias 47 and 50 are formed in separate steps (see, *e.g.*, col.5/ll.34-35). In the second process vias 47 and 50 are formed in a single operation (see, *e.g.*, col.5/ll.54-55). In the first process, because of the requirements to protect the bit, the vias 47 are formed first (see, *e.g.*, col.5/ll.25-27). Subsequent to forming vias 47, vias 50 are formed (see, *e.g.*, col.5/ll.35). Because in the first process Tehrani uses two separate steps to form vias 47 and 50, the etching step of vias 50 is customized so that it is safe enough that the vias 50 may extend outside the bit 41 without damaging the bit (see, *e.g.*, col.5/ll.25-38, 48-50). That is because the bit 41 is protected while vias 47 are formed (see, *e.g.*, col.5/ll.27-33), and the chemistries of the etching step of vias 50 are gentle enough not to damage or corrode the bit 41 (see, e.g., col.5/ll.48-50).

On the other hand, in the second process, Tehrani combines forming vias 47 and 50 in one single operation. Now Tehrani will use the same chemicals that were formerly used in the first process to form only vias 47 (see, *e.g.*, col.5/ll.27-33) to also form vias

50. To better protect the bit 41, Tehrani restricts forming the vias 50 so that the contacts may not extend outside the ends of the bit (see, *e.g.*, col.5/ll.58-62).

Looking at figure 7 it is easily seen why would Tehrani restrict vias 50 to not extend outside the ends of bit 41 in the second process. Vias 47 extend all the way down to wiring layer 13. Since in the second process Tehrani is using the same chemistry to etch both vias 47 and 50, if vias 50 were to extend outside the ends of the bit 41, then the etching step may undercut beneath the bit.

Regarding both processes, Tehrani teaches that the cap layer 45 is a dielectric layered system and he specifically refers to it as the dielectric cap layer 45 in his description of both processes (see, *e.g.*, col.5/ll.4 and col5/ll.57-58). This dielectric cap 45 completely seals the bit structure 41 and provides a barrier to moisture, oxidation, and corrosive agents (see, *e.g.*, col.5/ll.1-4 and figure 5). As he further explains, it is the first layer of the dielectric system that completely seals the bit structure 41 (see, *e.g.*, col.5/ll.4-8). This is also illustrated in figure 5, where Tehrani shows the cap layer 45 sealing the bit structure 41. Tehrani also sets forth the differences between the cap layer of the first and second processes, *i.e.*, in the first process the first layer of the dielectric cap is an insulating barrier and in the second process the first layer of the dielectric cap 45 is a conductive etch stop barrier layer (see, *e.g.*, col.5/ll.4-9, col.5/ll.55-58 and col.5/ll.67-col.6/ll.2).

Appellants conclusion that the etch stop barrier layer does not encapsulate the sidewalls of the bit because the vias 50 may not extend outside the bit is not described by Tehrani. What it is clearly described in Tehrani is the fact that first layer of the cap

layer 45 completely seals the bit 41 (see, *e.g.*, col.5/ll.4-8) and that in the second process this first layer is CrSi, which is a conductive material (see, *e.g.*, col.5/ll.55-58 and col.5/ll.67-col.6/ll.2).

The appellants argue:

The examiner relies on Tehrani's figure 6 as support for the assertion that Tehrani teaches selectively patterning the etch-stop layer so that edges of the layer extend out past the edges of the GMR bit 41 (see, e.g., fig. 6). Figure 6 applies only to Tehrani's dielectric barrier process and not to Tehrani's conductive barrier process. The appellants note that figure 6 illustrates only vias 47. Vias 50 are not present until next figure 7. In the first process, vias 47 and 50 are formed in separate steps (see, *e.g.*, col.5/ll.34-36), whereas in the second process, the vias are formed in a single operation (see, *e.g.*, col.5/ll.54-55). Accordingly, in the conductive barrier layer process, figure 6 does not apply.

The examiner responds:

Applicant's arguments above relate to limitations in claims 8-20. The arguments have been considered but are moot in view of the examiner's withdrawal of the rejection of these claims.

The appellants argue:

The examiner acknowledges that Tehrani does not specify the thicknesses of the etch-stop layer and the tantalum diffusion barrier. The examiner then uses Yue to provide the missing thicknesses and raised the issue of criticality. Neither Tehrani nor Yue recognizes the criticality of the thicknesses of either material. The thickness of the CrSi layer and/or Ta layer is important, as it relates to the resistivity of the material that is shunting the bit. If the materials are too thick, the bit is effectively shorted by the CrSi layer.

The examiner responds:

The examiner appreciates appellant's effort to establish the criticality of the claimed thicknesses. However, appellants' statements that the claimed thickness is important as it relates to the resistivity of the material fail to overcome the rejection of the claims. To be of probative value, appellants' assertion should be supported by actual proof.

The MPEP gives guidelines on how to demonstrate the criticality of a claimed range. See, *e.g.*, MPEP§716.02(d). As explained therein, the appellants should

compare a sufficient number of tests both inside and outside the claimed range to show the criticality of the range. The evidence relied upon should establish "that the differences in results are in fact unexpected and unobvious and of both statistical and practical significance." *Ex parte Gelles*, 22 USPQ2d 1318, 1319 (Bd. Pat. App. & Inter. 1992). The appellants, however, have failed to present any data showing that having a CrSi layer of about 300 angstroms and having a Ta layer of about 100 angstroms is critical. Due to the absence of said data, the examiner concludes that appellants' assertion that the claimed thicknesses are critical constitutes mere argument.

Therefore, since the appellants have failed to establish the criticality of the claimed thicknesses of the barrier layers, and since similar thicknesses have been used in similar processes in the art (see, *e.g.*, Yue/col.2/ll.40-42), and since the cited art shows all other limitations in the claims, it would have been obvious to one of ordinary skill in the art to use the claimed values in the device of Tehrani.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

An appeal conference was held on 11/14/2006 between Mr. Marcos D. Pizarro (Primary Examiner), Mr. Ricky L. Mack (Supervisory Patent Examiner), and Mr. Wael Fahmy (Supervisory Patent Examiner) as the conferees.

Respectfully submitted,

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